REMARKS:

Applicants have carefully studied the Non-Final Examiner's Action and all references cited therein. The amendment appearing above and these explanatory remarks are believed to be fully responsive to the Action. Accordingly, this important patent application is now believed to be in condition for allowance.

Applicants respond to the outstanding Action by centered headings that correspond to the centered headings employed by the Office, to ensure full response on the merits to each finding of the Office.

Claim Objections

Claim 24 stands objected to due to informalities.

Claim 24 has been amended to overcome the objections by the Office and is now believed to be in condition for allowance.

Claim Rejections – 35 U.S.C. § 103

Applicants acknowledge the quotation of 35 U.S.C § 103(a).

Claims 1-24 stand rejected under 35 U.S.C § 103(a) as being unpatentable over Applicants' Admitted Prior Art [hereinafter AAPA] in view of Park et al. [US 5,526,508 A; hereinafter Park].

Regarding independent claim 1, the Office states that the AAPA discloses a method for transferring information to a bus (i.e. Bus 106 of Fig. 1; See page 7, paragraph [0025], lines 1-3), comprising: receiving an indication (i.e. CPU_WR_COM or CPU_RD_COM) that information (i.e. CAD, CDW and CCO in Fig. 2-3) is to be transferred to a bus (i.e. Bus 106 of Fig. 1; See page 8, paragraph [0028]); reading a bus grant indication (i.e. indication on GNT/PARKING-GNT in Fig. 2; see page 9, paragraph [0029]); writing the information (i.e., said CAD, CDW and CCO) to a buffer (i.e. Two-Entry Buffer 202 of Fig. 2); and transferring the information (i.e. said information CAD, CDW and CCO in said Two-Entry Buffer) to the bus if the bus grant

indication (i.e. said GNT/PARKING-GNT) indicates that transfer of the information to the bus is allowed (See page 9, paragraph [0029]). The Office then states that AAPA does not teach writing the information to said buffer if the bus grant indication does not indicate that transfer of the information to the bus is allowed; and bypassing the buffer and said transferring the information to the bus if the buffer is empty and the transfer of the information to the bus is allowed.

The Office contends that Park discloses a method for a cache line replacing system (See Fig. 3 and Abstract), wherein said method (i.e. said method for cache line replacing system) for reducing latency in information transfers (See col. 3, lines 2-3) to a bus (i.e. CPU/Cache bus 31 of Fig. 3) including writing information (i.e. line of cache data) to a buffer (i.e. RD Buffer 36 of Fig. 3) if a bus grant indication does not indicate that transfer of the information to the bus is allowed (i.e. said CPU/Cache bus is not allowed to be used by memory read cycle during write back cycle of the steps 51 and 52 in Fig. 5, in other words, said CPU/Cache bus is occupied by said write back cycle; See col. 6, lines 11-14); and bypassing the buffer (See Title: bypassing said RD buffer) and transferring the information (i.e. said line of cache data) to the bus (i.e. said CPU/Cache bus) if the buffer (i.e. said RD buffer) is empty (i.e. said Buffer WT Reg counts 'zero'; See col. 5, lines 26-30) and transfer of the information to the bus is allowed (i.e. said CPU/Cache bus is allowed for memory read cycle after write back data having been stored in write-back buffer; See col. 3, lines 27-35, and col. 4, lines 31-46).

The Office concludes that it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said method step of transferring, as disclosed by Park, in said method, as disclosed by AAPA, for the advantage of providing a way that a device (i.e. CPU) can read said information (i.e. data) at high speed without loss of said bus bandwidth (i.e. memory bus bandwidth; See Park, col. 6, lines 30-31).

Applicants respectfully disagree with the finding of the Office.

The Office contends that Park discloses a method for a cache line replacing system (See Fig. 3 and Abstract), wherein said method (i.e. said method for cache line replacing system) for reducing latency in information transfers (See col. 3, lines 2-3) to a bus (i.e. CPU/Cache bus 31 of Fig. 3) including writing information (i.e. line of cache data) to a buffer (i.e. RD Buffer 36 of

Fig. 3) if a bus grant indication does not indicate that transfer of the information to the bus is allowed (i.e. said CPU/Cache bus is not allowed to be used by memory read cycle during write back cycle of the steps 51 and 52 in Fig. 5, in other words, said CPU/Cache bus is occupied by said write back cycle; See col. 6, lines 11-14). As such, the Office has concluded that the element of the present invention which states that, "writing information to a buffer if a bus grant indication does not indicate that transfer of the information to the bus is allowed", is equivalent to the Park reference in which the CPU/Cache bus is not allowed to be used by the memory read cycle during the write back cycle because the CPU/Cache bus is occupied during the write-back cycle.

Applicants point out that steps 51 and 52 of Fig. 5 illustrate that Park teaches storing write-back data in a write-back buffer and storing data in a read buffer until all the write-back data has been stored in the write-back buffer. As such, the indication used by Park to allow the transfer of information to the CPU/Cache bus is when all the write-back data has been stored in the write-back buffer. By contrast, in the case of the present invention, the indication to allow transfer of information to the bus is the bus grant indication. The bus grant indication in accordance with the present invention indicates that the specific information which is requesting transfer to the bus has been allowed access to the bus. It is not based upon the fact that all the write-back data has been stored in the write-back buffer, but rather that an indication has been made by a bus grant indication that specific information is allowed to be transferred to the bus. As such, Park does not describe a method in which information is stored in the buffer if the bus grant indication does not indicate that transfer of the information from the device to the bus is allowed, but rather describes a method in which information is stored in the read buffer during the time the write-back data is being stored in the write-back buffer.

The Office contends that Park teaches bypassing the buffer (See Title: bypassing said RD buffer) and transferring the information (i.e. said line of cache data) to the bus (i.e. said CPU/Cache bus) if the buffer (i.e. said RD buffer) is empty (i.e. said Buffer WT Reg counts 'zero'; See col. 5, lines 26-30) and transfer of the information to the bus is allowed (i.e. said CPU/Cache bus is allowed for memory read cycle after write back data having been stored in write-back buffer; See col. 3, lines 27-35, and col. 4, lines 31-46).

In the statement by the Office above, the Office fails to include the complete element of the claim which states that, "the bus grant indication indicates that transfer of the information to the bus is allowed". The Office has not addressed the use of the bus grant indication to indicate that transfer of information to the bus is allowed. As such, the Office contends that the statement, "transfer of the information to the bus is allowed", is equivalent to the claim language which states, "the bus grant indication indicates that transfer of the information to the bus is allowed". Just because the CPU/Cache bus is idle after write-back data has been stored in the write-back buffer, this does not mean that transfer of information to the bus is allowed as claimed by the present invention. The claim must be considered as a whole and in doing so it is clear that the bus grant indication is the means through which the system of the present invention indicates that the transfer of information to the bus is allowed. Simply because the bus is idle does not mean that transfer of said information to the bus is allowed, there may be other bus requests waiting to be serviced. The bus grant indication in accordance with the present invention indicates that the specific information which is requesting transfer to the bus has been allowed access to the bus. It is not simply that the bus is idle, but that an indication has been made by a bus grant indication that specific information is allowed to be transferred to the bus. This "allowance of transfer" is not equivalent to the bus being idle and "available for transfer".

Additionally, the Park reference does not discuss the use of any type of bus grant request system to track the status of the CPU/Cache bus. In the Park reference, the CPU/Cache bus is always available for access by the cache buffer or the memory bus. Park does not discuss the need for a bus grant to access the bus because apparently the bus is always available when it is not being used. It can be inferred that the CPU/Cache bus is a dedicated bus and therefore bus grant requests and the issuance of grants are not necessary with the Park system.

Another issue before the Office is whether it would have been obvious to combine the references without having access to the application that is under examination to arrive at the claimed invention. In support of the combination of references, the Office states that it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said method step of transferring, as disclosed by Park, in said method, as disclosed by AAPA, for the advantage of providing a way that a device (i.e. CPU) can read said information (i.e. data) at high speed without loss of said bus bandwidth (i.e. memory bus bandwidth; See

Park, col. 6, lines 30-31). Applicants respectfully disagree with the determination by the Office regarding the combination of references.

Park teaches transferring information to the bus when the buffer is empty and the bus is "available", not that the transfer of the information to the bus is "allowed", which are two different things as explained above. The AAPA teaches the use of a bus grant indication to indicate that transfer of the information to the bus is "allowed". The Park reference does not provide any motivation to substitute the use of a bus grant indication to indicate that transfer of the information to the bus is allowed. The Park reference does not address the need for any type of grant request indicators for the CPU/Cache bus. As such, the Applicants contend that the Office has improperly used the instant application as a basis for the motivation to combine or modify the prior art to arrive at the claimed invention.

To establish a *prima facie* case of obviousness, the prior art must cited must teach or suggest all the claim limitations. Neither the Park et al. reference nor the Applicants' Admitted Prior Art teach or suggest the step of transferring the information to the bus if the buffer is empty and the bus grant indication indicates that transfer of the information to the bus is allowed. Therefore, a *prima facie* case of obviousness has not been established because the cited references fail to disclose all the elements of the Applicants' invention.

Regarding independent claim 9, the Office states AAPA Discloses a bus interface unit (i.e. convention BIU 105 in Fig. 1; pg. 7, paragraph [0023], lines 1-4) in information transfers from a device (i.e., CPU 101 of Fig. 1) to a bus (i.e., Bus 106 of Fig. 1; see pg. 7, paragraph [0025], lines 1-3), comprising: a buffer (i.e., Two-Entry Buffer 202 of Fig. 2) having inputs coupled to the device (i.e., said CPU; see Fig. 1-2, pg. 7, paragraph [0025], lines 1-3) and logic (i.e., control logic 201 of fig. 2) configured to receive an indication (i.e., CPU_WR_COM or CPU_RD_COM) from the device (i.e., said CPU) that information (i.e, CAD, CDW, and CCO in Fig. 2-3) is to be transferred to the bus (i.e., said Bus; See page 8, paragraph [0028]), read a bus grant indication (i.e., indication on GNT/PARKING-GNT in Fig. 2; pg. 9, paragraph [0029]), and cause the information (i.e., said CAD, CDW, and CCO) to be stored in the buffer (i.e., said Two-Entry Buffer), and to be transferred from the buffer (i.e., said Two-Entry Buffer) to the bus if the bus grant indication (i.e., said GNT/PARKING-GNT) indicates that transfer of the information from the buffer to the bus is allowed (pg. 9, paragraph [0029]).

The Office goes on to state that AAPA does not teach said logic being configured to cause the information to either be stored in the buffer if the bus grant indication does not indicate that transfer of the information from the device to the bus is allowed, or be transferred from the device to the bus, thereby bypassing the buffer, if the buffer is empty and the transfer of the information to the bus is allowed. However, the Office concludes that Park discloses a cache line replacement apparatus (Fig. 3 and Abstract), wherein a bus interface unit (i.e., said cache line replacement apparatus) for reducing latency in information transfers (col. 3, lines 2-3) from a device (i.e., Main Memory 100 of Fig. 3) to a bus (i.e., CPU/Cache bus 31 of Fig. 3) including logic (i.e., MUX 38 and Buffer WT Reg 37 in Fig. 3) configures to cause information (i.e. line of cache data) to either be stored in a buffer (i.e. RD buffer 36 of Fig. 3) if the bus grant indication does not indicate that transfer of the information from the device to the bus is allowed (i.e. said CPU/Cache bus is not allowed to be used by memory read cycle during write-back cycle of the steps 51 and 52 in Fig. 3, in other words, said CPU/Cache bus is occupied by said write back cycle; see col. 6, lines 11-14), or be transferred from the device (i.e., said Main Memory) to the bus (i.e., said CPU/Cache bus), thereby bypassing the buffer (See Title; bypassing said RD buffer); if the buffer (i.e., said RD buffer) is empty (i.e., said Buffer WT Reg counts 'zero'; see col. 5, lines 26-30) and transfer of the information to the bus is allowed (i.e., said CPU/Cache bus is allowed for memory read cycle after write-back data having been stored in write-back buffer; See col. 3, lines 27-35, and col. 4, lines 31-46).

The Office concludes that it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said logic (i.e., MUX and Buffer WT Reg), as disclosed by Park, in said logic (i.e., Control Logic), as disclosed by AAPA, for the advantage of providing a way that said device (i.e., CPU) can read said information (i.e., data) at high speed without loss of said bus bandwidth (i.e., memory bus bandwidth; see Park, col. 6, lines 30-31).

Applicants respectfully disagree with the finding of the Office. As detailed with regard to independent claim 1, the claim of the present invention must be considered as a whole and in doing so it is clear that the bus grant indication is the means through which the system of the present invention indicates that the transfer of information to the bus is allowed. The bus grant indication in accordance with the present invention indicates that the specific information which is requesting transfer to the bus has been allowed access to the bus. It is not based upon the fact

that all the write-back data has been stored in the write-back buffer, but rather that an indication has been made by a bus grant indication that specific information is allowed to be transferred to the bus. For the reasons cited above, Applicants contend that Park does not describe logic being configured to cause information to either be stored in the buffer if the bus grant indication does not indicate that transfer of the information from the device to the bus is allowed, or be transferred from the device to the bus, thereby bypassing the buffer, if the buffer is empty and the transfer of the information to the bus is allowed.

The Office concludes with regard to independent claim 9 that it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said logic, as disclosed by Park, in said logic as disclosed by AAPA, for the advantage of providing a way that said device can read information at high speed without loss of said bus bandwidth.

The Applicants respectfully disagree with the Office's conclusion regarding the motivation to combine the references as suggested by the Office. As previously detailed with regard to independent claim 1, Applicants contend that the Park reference does not provide any motivation to substitute the use of a bus grant indication to indicate that transfer of the information to the bus is allowed. The Park reference does not address the need for any type of grant request indicators for the CPU/Cache bus. As such, the Applicants contend that the Office has improperly used the instant application as a basis for the motivation to combine or modify the prior art to arrive at the claimed invention.

Regarding independent claim 19, the Office states that AAPA does not teach said information to be transferred from the device to the bus is stored in the buffer if a bus grant indication generated by the bus arbiter indicates that the bus is unavailable for the transfer, or the bus grant indication indicates that the bus is available for transfer of the information to the bus, and a buffer bypass circuit for reducing latency in information transfers to the bus comprising: a multiplexer having first inputs coupled to inputs to the buffer, second inputs coupled to outputs of the buffer, outputs coupled to the bus, and at least one select input for selectively coupling either the first or the second inputs to the outputs; and logic configured to provide control information to the at least one select input such that the first inputs are coupled to the outputs of the multiplexer if the buffer is empty and the bus is available for transfer of the information to the bus.

However, the Office goes on to state that Park discloses a cache line replacement apparatus (see Fig. 3 and Abstract), wherein information (i.e., line of cache data) to be transferred from device (i.e., Main Memory 100 of Fig. 3) to a bus (i.e., CPU/Cache bus 31 of Fig. 3) is stored in a buffer (i.e., RD Buffer 36 of Fig. 3) if a bus grant indication generated by a bus arbiter (i.e., means for controlling cache line replacing cycles; See abstract) indicates that the bus is unavailable for the transfer (i.e., said CPU/Cache bus is not allowed to be used by memory read cycle during write back cycle of the steps 51 and 52 in Fig. 3, in other words, said CPU/Cache bus is occupied by said write back cycle. See col. 6, lines 11-14), or the bus grant indication indicates that the bus is available for transfer of the information to the bus (i.e., said CPU/Cache bus is allowed for memory read cycle after write-back data having been stored in write-back buffer; See col. 3, lines 27-35, and col. 4, lines 31-46), and a buffer bypass circuit (i.e., said cache line replacement apparatus) for reducing latency in information transfers (See col. 3, lines 2-3) to the bus (i.e., said CPU/Cache bus) comprising: a multiplexer (i.e., MUX 38 of Fig. 3; see col. 4, lines 40-46) having first inputs (i.e., input of said MUX being coupled to Memory Bus 32 in Fig. 3) coupled to inputs to the buffer (i.e., said RD Buffer being coupled to said Memory Bus in Fig. 3), second inputs (i.e., input of said MUX being coupled to Bus Line 33 in Fig. 3) coupled to outputs of the buffer (i.e., output of said RD Buffer), outputs coupled to the bus (i.e., output of said MUX being coupled to CPU/Cache bus 31 in Fig. 3), and at least one select input (i.e., input from Buffer WT Reg 37 in Fig. 3) for selectively coupling either the first or the second inputs to the outputs (See col. 3, lines 27-35); and logic (i.e. MUX 38 and Buffer WR Reg 37 in Fig. 3) configured to provide control information (i.e. MUX control information from said Buffer WT Reg) to the at least one select input (i.e., input of said MUX being coupled to said Memory Bus) such that the first inputs (i.e., input of said MUX being coupled to said Memory Bus) are coupled to the outputs of the multiplexer (i.e., output of said MUX being coupled to said CPU/Cache Bus) if the buffer (i.e., said RD Buffer) is empty (i.e. said Buffer WT counts 'zero'; See col. 5, lines 28-30) and the bus is available for transfer of the information to the bus (i.e. said CPU/Cache is idle after write-back data having been stored in write-back buffer (See col. 3, lines 27-35, and col. 4, lines 31-46).

Applicants respectfully disagree with the conclusion of the Office. Claim 19 of the present invention includes, "at least one select input for selectively coupling either the first or the second inputs to the outputs; and logic configured to provide control information to the at least

one select input such that the first inputs are coupled to the outputs of the multiplexer if the buffer is empty and the bus is available for transfer of the information to the bus." As such, the control information couples the first inputs of the multiplexer to the outputs of the multiplexer, which are coupled to the bus, if the buffer is empty and the bus is available for transfer of the information to the bus. The Office states that Park teaches that the bus is available for transfer of the information to the bus, as supported by col. 3, lines 27-35, and col. 4, lines 31-46, in which the CPU/Cache bus is idle after write-back data having been stored in write-back buffer. As detailed with regard to independent claim 1, just because the CPU/Cache bus is idle after write-back data has been stored in the write-back buffer, does not mean that the bus is available for transfer of "the" information to the bus, as claimed by the present invention. The availability of the bus is determined by the grant indication of the present invention. The claim must be considered as a whole and in doing so it is clear that the bus grant indication is the means through which the system of the present invention indicates that the bus is available for transfer of the information to the bus. It is not simply that the bus is idle, but that an indication has been made by a bus grant indication that the bus is available for the transfer of identified information to the bus. For the reasons cited above, Applicants contend that Park does not describe logic configured to provide control information to the at least one select input such that the first inputs are coupled to the outputs of the multiplexer if the buffer is empty and the bus grant indication indicates that the bus is available bus is available for transfer of the information to the bus.

The Office concludes that it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said buffer bypass circuit, as disclosed by Park, in said logic (i.e., Control Logic), as disclosed by AAPA, for the advantage of providing a way that said device (i.e., CPU) can read said information (i.e. data) at high speed without loss of said bus bandwidth (i.e., memory bus bandwidth; See Park, col. 6, lines 30-31).

The Applicants respectfully disagree with the Office's conclusion regarding the motivation to combine the references as suggested by the Office. As previously detailed with regard to independent claim 1, Applicants contend that the Park reference does not provide any motivation to substitute the use of a bus grant indication to indicate that the bus is available for transfer of the information to the bus. The Park reference does not address the need for any type of grant request indicators for the CPU/Cache bus. As such, the Applicants contend that the

Office has improperly used the instant application as a basis for the motivation to combine or modify the prior art to arrive at the claimed invention.

For the reasons cited above, Applicants believe that independent claim 1 is patentable over Applicants' Admitted Prior Art in view of Park et al. and is believed to be in condition for allowance.

Claims 2-8 are dependent upon claim 1, and are therefore allowable as a matter of law.

For the reasons cited above, Applicants believe that independent claim 9 is patentable over Applicants' Admitted Prior Art in view of Park et al. and is believed to be in condition for allowance.

Claims 10-18 are dependent upon claim 9, and are therefore allowable as a matter of law.

For the reasons cited above, Applicants believe that independent claim 19 is patentable over Applicants' Admitted Prior Art in view of Park et al. and is believed to be in condition for allowance.

Claims 20-24 are dependent upon claim 19, and are therefore allowable as a matter of law.

If the Office is not fully persuaded as to the merits of Applicant's position, or if an Examiner's Amendment would place the pending claims in condition for allowance, a telephone call to the undersigned is requested.

Respectfully Submitted,

1/8/07
Date

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